

Hogthrob Prototype Platform



M.Sc. Thesis by Martin Leopold

Hogthrob

Sensor network for sow monitoring

This thesis is placed in the context of the Hogthrob project: a 3 year research project with partners from:

- DTU
- KVL
- DIKU

The goal is to build a sensor network for sow monitoring.

Sow monitoring today:

- RF-ID ear tags
 - identification for feeding-station
 - estrus detection (boar visit)

Hogthrob:

- Replace ear tag with sensor node
- Define a sensor node that fit the requirements

Approach:

- Design a prototype to explore designspace

Key challenges:

- How to detect estrus?
- How to evaluate design choices?

Goals

Sensor network for sow monitoring

- Functionalities
 - Tracking
 - Detection Heat Period
- Low cost (~ 1 EUR)
- Low energy (2 years)



The real Hogthrob

Challenges

1. Is there a sensor node that fit the req.?
 - The current generation of sensor nodes a built as "one-node-fits-all". This strategy is has drawbacks:
 - The hardware is fixed
 - The price is too high
 - The performance is limited (formfactor, power).
 - => we need a sensor node built for this application

2. How do we meet the requirements of the app.?
 - During the design of our sensor node we need a systematic approach to evaluate design choices.

In particular, how do we evaluate the power consumption of a sensor node as a part of the design process (before it is built)

Power estimation strategies

1. Direct measurements
 - Input: real
 - Program: real
2. Simulation
 - Input: synthetic
 - Program: synthetic, derived, real

New approach

Hybrid using the HogthrobV0 platform

- Use hardware simulation (FPGA)

What's new?

- Allows exploring every aspect of the design space
- Simulation in situ

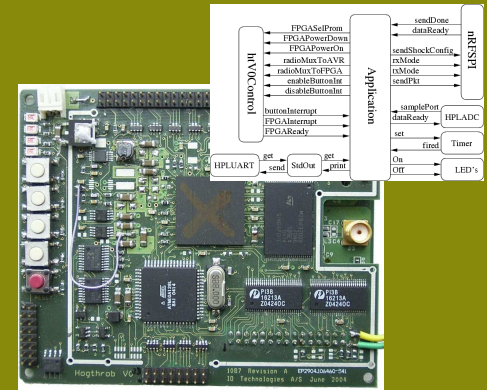
Prototype Platform: HogthrobV0

The prototype platform (hogthrobV0) is built as part of the research project. Through my thesis work I took part in designing this platform.

HogthrobV0 is not a sensor node, and does not share the properties of a sensor node (price, power, etc.)

It features an FPGA an a simple microcontroller. The microcontroller functions as an external timer and A/D converter to the FPGA. Also it will serve as the main processor in the beginning and gradually software will be moved to a microprocessor in the FPGA.

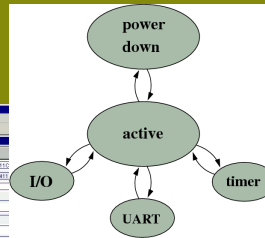
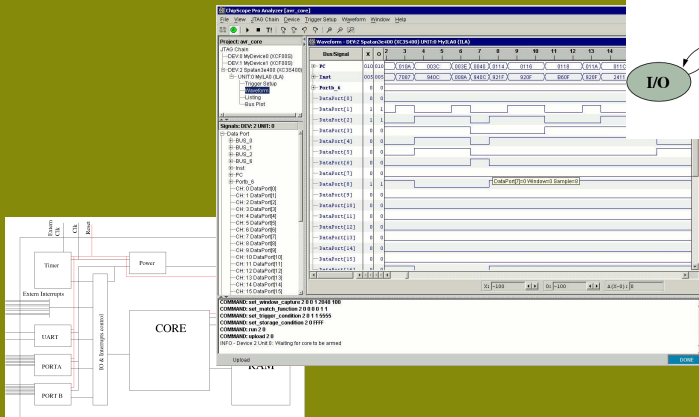
- FPGA: Xilinx Spartan3
- MCU: Atmel ATmega128l
- Radio: Nordic VLSI nRF2401
- Sensors:
 - Analog Devices ADXL320
 - ST Micro: ST-LIS3L02DS
 - Nimbus processor core (ATMega compatible)



Proof of concept

I have implemented a proof of concept of this new approach:

1. The Nimbus core is placed in the FPGA
2. An activity trace is captured
3. Using a power model this is mapped to the power consumption that could be expected if this was implemented as a chip



Nimbus processor core

Activity trace

Power model

What's next?

This technique is a proof of concept and must be developed further to provide a working technique. It is the topic of my Ph.D. to develop the ideas presented here.

Field experiments

To get a feel of the kind of data that can be expected a first experiment was carried out.

5 sows were mounted with a sensornode and collected data for 30 days in a stable. 4 cameras were mounted to monitor the sows

